

ICU 2003 Specetra Submitted Issues

- Title:** 'Buried resistor capabilities.'

Description: "Buried resistor capabilities. Better way to control routing (critical routing diff pairs). All around better control over routes.'
- Title:** 'Include recent feature conflicts in the status report columns'

Description: 'The status report is the most widely used tool to analyze the auto router progress and where problems occur and now at the end of the report we have the following:
| Stub Violations: 25
| Net Order Violations: 78
| Diff pair Uncoupled Length Violations: 16
| Diffpair Phase Tolerance Violations: 15
| Total layerset violations: 16
| Total layerset violations (exclude Fanout/Stagger): 14
We know that we are in trouble but have no idea how we got there unless we sit and watch it run. Would be helpful to include man/actual ratio as a column so we could see how that progresses downward (hopefully) during the routing.'
- Title:** 'Provide cost and tax for cross-talk length and topology '

Description: 'provide cost and tax for cross-talk length and topology conflicts. Similar benefit to the current use of cross and squeeze.'
- Title:** 'Tandem Diff pairs.'

Description: 'Tandem Diff pairs, Need the ability to auto and manually control and route tandem diff pairs. '
- Title:** 'Command to make every net on board as short as possible'

Description: 'Command to make every net on board as short as possible while maintaining rules. Possibly with options such as removing vias. Provide a faster more effective alternative to the do file sequence "wringer" needs to fix (WHEN EASY). Frees up real estate for increased completion and length rule use. In general length reduction improves signal integrity as well improving customer acceptance of auto routing as compared to manual routing. Help address the "we want it as short as possible" This can follow the model of what was done on miter in 15.0 '
- Title:** 'Detailed topology from/to order and lengths'

Description: 'Report selected up to a definable max pins in a net (default 20) showing: 1. the routing order of the from to s with each from/to Manhattan length & required and the topology rules and order rules that Specetra is applying to define that required order. Fromto order that is Specetra default should be so flagged. The length rules that are being applied to each from to and stub rules to stubs 2.The actual order details and lengths flagging the errors in both order and length if any again with Manhattan required and actual length details including stub. Note:virtual pins T junctions and via T s to be included. Available by queued request while the auto router is running for what is selected at that time. Used to sort out user/Specetra misunderstandings in multi rule topology length hierarchical and over lay resolution problems in both the planning and actual routing stage. Used to resolve impossible customer rule requirements Used to satisfy the customer that the requirements are met.
- Title:** 'Net/class/group/group set Cost/Tax layer:'

Description: ' This allows use layer combined with length cost by class to use the preferred layer set and minimal straps on the ("only when necessary to not fail"). This requirement is often expressed as mildly preferred - preferred - and only to avoid failure. Useful to optimize bga access/channel utilization where the current hard layer rules are unbalanced.'

8. **Title:** 'Net/class/group/group set Keepin and keepout:'

Description: 'By defining a keepout that only effects the specified net/class/group/group set provides guidance to the autorouter to keep sets of routing in or out of specified areas. This allows control of high speed nets in pairs/bundles far beyond the current fence and temp keepout select. examples: Certain Nets cannot cross power moats on adjacent layers. Certain nets must be kept within/outside the area of a specified gnd plane on an adjacent layer. Certain sets of nets should go out and around congested areas to avoid noise and solve congested routing issues'

9. **Title:** 'Fence by net (single net, group, class or layer)'

Description: 'It would be nice if there was a way to have fences that a particular class, net, group of nets would obey. This would allow a bus to follow the same general path or avoid a specific area. Also it should be easier to implement a fence by layer. Usage area: Routing and keeping signals in an area without worrying other signals.'

10. **Title:** "Specetra to Allegro translation rounding errors"

Description: 'Can you make it so there is no rounding errors coming back from SPECCTRA into ALLEGRO. I get a little surprised when I see line to line errors when I come back into Allegro.'

11. **Title:** 'Understanding Via Effects'

Description: 'For high-speed designs that span package and PCB domains timing margins are commonly shrinking to the 10's of picoseconds. It is expected that as the percentage of signals in high-speed designs that fall into this category increase it will cause a trend where users move from length-based calculations to handling interconnect purely in terms of time. This has already happened at many companies were time based rules have been used on production boards for over five years. Time based rule entry can improve accuracy in the handling of stripline vs. microstrip as well as signals that traverse multiple layers of PCB as well as packaging stack ups (e.g. Flip-Chip package-on-board *.mcm on *.brd). As the accuracy of all PCB structures become more critical the effect of every via structure MUST have better representation during simulation and routing. The router must understand the load and stub effects that a via has on the timing of a route.'

12. **Title:** 'Understanding Voltage Plane Effects'

Description: 'Currently the tool set does a very poor job of understanding how power flows through a board. Because of this the tool set ignores many important effects to the signal integrity as well as the timing of the power system. The old notion of a power plane with one voltage hidden from the routing layers by a ground plane is dead! In high-speed systems if the voltage plane effects are ignored the system will not function (or best case not function reliably). Thus the router must take into account the effect of routing traces that reference power planes change between power and ground reference planes jump plane splits and jump between different ground planes in the stack up.'

13. **Title:** "'DO" Language Enhancements'

Description: 'The DO language used to control Specetra is an undocumented and unsupported language. This is unacceptable. This language is so unsupported that system variables have been known to change type! When this was reported to Cadence they could not even give a time period for resolution they just recommended not using DO files. This is completely unacceptable. The DO Language should be brought up to date and include the following functionality:

- 1) ADDED LANGUAGE CONSTRUCTS Real language constructs such as SUBROUTINES ELSEIF DO...WHILE and/or CASE statements should be added.
- 2) LOCAL AND GLOBAL VARIABLES The concept of local and global variables should be included into the language.

- 3) LANGUAGE OPERATORS FOR STATISTICS The language operators should be expanded to include the ability to do statistical analysis with the systems variables.
- 4) SYNTAX CHECKING Syntax checking should flag errors and give reasonable feed back as to their origin (i.e. the line numbers). This could be accomplished with a good DO

14. Title: 'Layer Count Study (Layer Cloning)'

Description: 'While attempting to route a given board engineering usually starts with a 'best guess' as to how many routing layers will be needed to route the board. This is becoming increasingly more difficult to estimate with today's high-speed designs. All too often engineering spends hour upon hour trying to get a board to route only to find out that what is needed is more routing layers! There currently exists NO WAY to simply add two more layers in Allegro/Specetra for the purpose of conducting routability studies. Adding layers to the StackUp in Allegro at this stage of the game is a very complicated task at best. It's totally manual wasting great amounts of time as well as being quite prone to errors. There should be a straightforward way to perform routing studies in order to determine the total number of layers needed to route a board. Cadence must add support into Specetra and its (DO) language in order to support adding of these virtual layers on the fly during routing. This could be accomplished

15. Title: 'STUCK-IN-THE-BOX Routing'

Description: 'Specetra should never use the box formed by a driver/receiver pin pair to contain routing for nets with timing related rules assigned. A great example of the Stuck-in-the-box routing problem is found when implementing a Phase Locked Loop (PLL) feedback net that is routed between two pins on a device that are 200 mils apart. If the RELATIVE_PROPAGATION_DELAY rule attached to the feedback net calls for 24 inches of etch the router will attempt to put 24 inches of etch inside a box with 200x1 mil dimensions. As one might imagine the artificial restriction that the router has placed on itself makes the problem unsolvable. In most cases the router will simply not make these connections or will fail miserably in its attempt. Thus leaving the problem to be solved by the designer after the rest of the board has been routed. The only solution is to hand route these types of nets before sending the board to the router adding time to schedules and possibly causing artificial barriers. This simple problem when app

16. Title: 'Bi-directional rule passing and support.'

Description: 'All of work has been done over the past few years to align the Specetra and Allegro rule sets this is great but there are still rules that are not treated properly during the translations to and from. I.E. Areas! but there are more than that. The tools need to treat the rules the same no matter what GUI I am using to do the inter connect!!!! The Specetra tool also needs to pass the rules back to allegro it is unacceptable for a designer to change a rule in Specetra bring the design back to allegro and get DRC s and then have to update the rule manually in allegro to get rid of the DRC s. This is duplication of effort!!! and costs us time and money!!'

17. Title: 'Component placement UI Improvements'

Description: 'I would like to see an Active-X step by step guide in a flow like presentation much like the project manager; as an interface that would drive the workings of component placement. I feel that either that I would always have to use the component placement tools to be good at it (efficient) or it is too cumbersome to use making it a core deficiency of the UI or lack thereof.'

18. Title: 'Passing clearance rules for Constraint areas'

Description: 'When constraint areas are used in Allegro only 1 set of rules are passed to Specetra instead of all the rules for that constraint area. '

19. Title: 'Methodology/mechanism for concurrent routing of a single dsn.'

Description: 'Because we often can no longer fully auto-route many of our complex designs we are forced to combine manual route efforts for some sections of a board with auto-routing

other sections of the same board. Additionally the manual routing may be divided among multiple people. We need a mechanism that will automatically evaluate all of the completed .w/.rte files that were separately concurrently created and then combine them for one update to the .dsn. The combine needs to be intelligent and eliminate and/or notify of any conflicts auto-eliminate any duplicated routing and be able to repair conflicts/reconnect wires when possible.'

20. Title: 'Need better complex geometric bus auto-routing capability.'

Description: 'The current bus auto-routing schemes within Specctra are inadequate for many non-conventional/geometrically complex busses. Need the ability to define a set of nets as bus and then route them on one predefined signal layer with no vias(except fanout). The nets that comprise the bus may come from a bga on one end and go to a VHDM connector on the other. Many turns may be required in order to complete the route. The routing will also need to conform to region and length/timing rules.'

21. Title: 'Better performance for designs with positive shapes.'

Description: 'Graphics performance for designs with many and/or large positive shapes is extremely poor. Screen redraws zooms etc... are very slow.'

22. Title: 'Areafill Transfer from Allegro'

Description: 'Please let areafills transfer properly between Specctra and Allegro.'
There should be no conflicts created as result of the transfer. If there are no DRCs in Allegro, there should be no conflicts in Specctra and vice-versa.

23. Title: 'Min Length/Elongation Gap Rules ignored for same-net'

Description: 'When Specctra adds length to satisfy min length requirements it does not honor the gap rules against itself/same-net. Additionally the conflict checking mechanism should have an option for checking same-net gap rule violations.'

24. Title: 'Ability to import per layer routing constraints from Allegro'

Description: 'Ability for Specctra to understand physical constraint areas as defined in Allegro. I can set up Allegro such that certain nets will only be allowed in certain areas on a per-layer basis but that information does not translate to Specctra. This forces significant additional work and a piecemeal approach to create the equivalent constraints for auto routing in Specctra.'

25. Title: 'True Diagonal Layer Routing'

Description: 'Give Specctra true diagonal layer routing capability.'